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A Reconfigurable Modular Microelectrode Array Platform for Fast Prototyping of Implantable Closed-Loop Neuromodulation Medical Devices

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***Abstract*—Developing implantable, closed-loop neuromodulation devices demands seamless integration of neuroscience discovery, algorithm design, and ultra-low-power hardware—an effort that traditionally stretches across many years and multiple specialist teams. Existing commercial or open-source electrophysiology tools do not offer the broad flexibility desired to enable rapid testing of custom stimulation paradigms and closed-loop algorithms, slowing the path from bench-top insight to patient-ready silicon. To address this we present a flexible platform that integrates four interoperable modes: (1) Experimental validation - for neuroscientists to explore new stimulation protocols and test their efficacy; (2) Software development - to enable real-time closed-loop algorithm testing; (3) Hardware development - for translation of proven software code into FPGA-accelerated, power-efficient hardware; (4) ASIC validation - for post-silicon performance testing before deployment in chronic studies. This modular architecture enables parallel, cross-functional collaboration, reduces design spins, and lowers entry barriers for labs lacking end-to-end neuromodulation infrastructure. Preliminary in-vitro results from human brain tissue using microelectrode arrays demonstrate reliable operation, validating the system. By streamlining the transition from neuroscience insight to implant-grade ASIC, our system accelerates therapeutic device development and opens new avenues for fundamental investigations of brain function.**

***Index Terms*—microelectrode array, bioelectronics, neural interfaces, implantable ASICs, closed-loop neuromodulation**

I. Introduction

The journey of developing implantable, closed-loop neuromodulation devices that would be capable of treating otherwise intractable neurological disorders is a lengthy and highly iterative process. A successful effort requires close collaboration among neuroscientists, clinicians, biomedical engineers, electrical and computer engineers, and integrated-circuit (IC) designers. Only a few laboratories in the world would possess the full complement of resources and expertise needed to span this highly multidisciplinary skillset. Mastery of neuroscience, clinical protocols, software programming, and hardware design often takes years to cultivate. Translating that collective knowledge into rigorously tested prototypes demands several more. These challenges help explain why the path from promising neurophysiological insights to a patient-ready, miniaturized implantable chip remains protracted and elusive.

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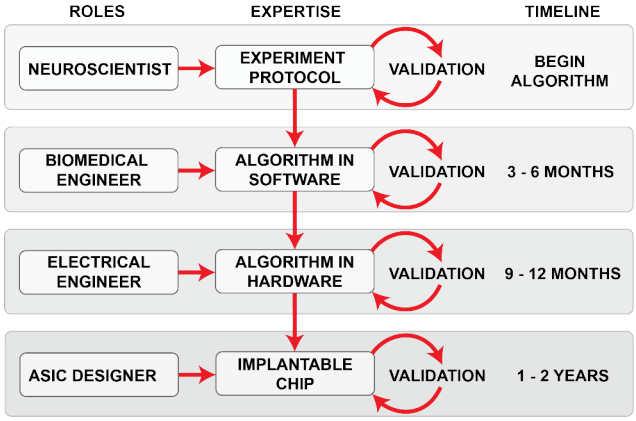

Fig. 1. The path from discovering neuro-physiological insights for a disease model to developing implantable chips with closed-loop algorithms takes several months to years and requires extensive validation from a cross-functional team of varied skillset

Closed-loop neuromodulation research needs hardware that can perform extracellular electrophysiology to record signals, extract insights from the data and modulate activity by stimulation. Over the past decades, several commercial and research-grade systems have attempted to fulfill this need. While some only allowed recording [1][2], others offered limited stimulation capability [3][4], and few advanced systems had limited flexibility to interface and test custom algorithms and circuits [5]. This restricted their use beyond neuroscience experiments. Open-source systems such as NeuroRighter [6] and OpenEphys [7] improved access, but the lack of reliable electrical stimulation capability restricted their usefulness for closed-loop algorithm research. The ONIX Platform has shown promising results but lacks the flexibility to test custom algorithms in hardware [8]. To fill that gap our team has developed solutions [9], including the OpenMEA [10] — an open source platform for closed-loop bioelectronics research. Building upon that foundation, we have enhanced its capabilities to create a flexible platform that lets researchers plug in

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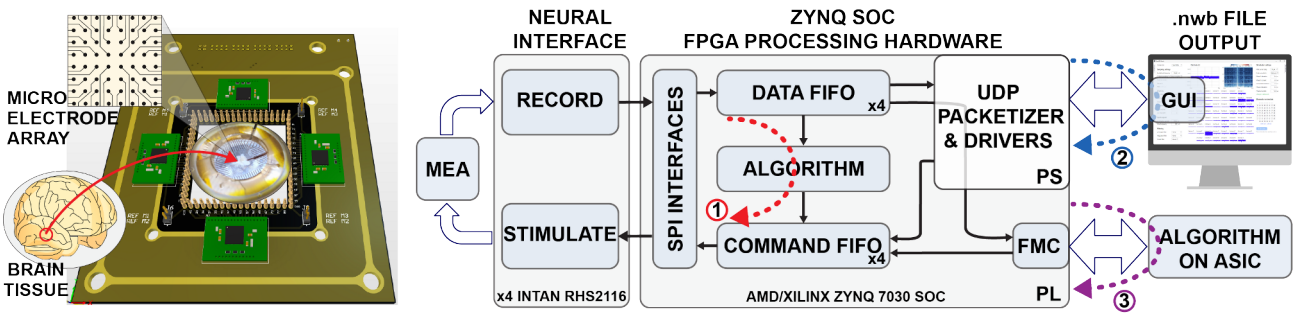

Fig. 2. System overview showing (a) Custom designed neural interface headstage PCB with a central cavity to interface with MEAs; (b) SoC-FPGA processing system; (c) Graphical user interface (GUI); (d) FMC connection for ASIC interface. 3 different ways to test closed-loop algorithms is shown. (1) In hardware on the FPGA, (2) in Software on the PC or as a module developed within the GUI, and (3) On external ASIC interfaced with the processing hardware.

their custom algorithms or circuits and test under experimental conditions that remain identical from bench-top experiments all the way to implant-ready silicon, which existing tools don't provide.

The updated platform supports four independent but interoperable work modes (Fig 1). (1) Experimental validation: neuroscientists can test new protocols that evolve into insights for closed-loop algorithms. (2) Software development: neuroscientists and biomedical engineers can script new protocol modules in Python or C, quickly deploy algorithms to gain insights during experiments, and conduct studies to validate their results. (3) Hardware development: Electrical and Computer engineers can adapt algorithms validated in software into low-power hardware optimized models to be deployed on FPGAs and run real-time closed-loop tests, and debug before committing to costly chip fabrication. (4) ASIC validation: To ensure the fabricated chip can work during experiments and meet specifications under identical test conditions. Besides this, our platform offers the capability to run any combination of hardware or software simultaneously during in-vitro experiments for parallel development. This modular workflow bridges skill gaps across teams, minimizes design spins, and accelerates delivery of thoroughly validated, implant-grade neuromodulation chips.

II. System Overview

The platform consists of several subsystems as shown in Fig. 2. It includes a Neural Interface Headstage PCB with 60 channels (expandable to 64), that is custom designed to interface with a Microelectrode Array (MEA) for recording neural signals from brain tissue and stimulate with programmable biphasic pulses. The recorded data is streamed to a Processing Hardware that packetizes and sends it to a PC for display on a GUI. Stimulation parameters can be setup on the GUI and are sent to the processing hardware for electrical stimulation. A parallel path to interface the processing hardware to another FPGA or an ASIC is provided using FMC connector. Fig. 3 shows the overall experimental setup. Below sections explain the details of each subsystem

A. Neural Interface Headstage

The headstage comprises of a custom PCB that has a central cavity with spring-loaded pogo pins that makes contact with a perforated Microelectrode array (pMEA). Four Neural Interface modules are placed on top in the cardinal directions around the cavity and interface with the electrodes on the pMEA. Each module has an Intan RHS2116 - A 16-channel low-noise biopotential amplifier and stimulation chip. We can achieve sampling rates of upto 35.9 KS/s across all 60 channels with an input referred noise (IRN) of 2.4uVrms. These modules are replaceable if they fail during experiments. The headstage is shielded on the top using copper plate with a similar cavity, and covered by a 3D printed enclosure and connected to ground to reduce EM interference. The Neural Interfaces communicate with the processing hardware using LVDS signaling, which improves signal integrity over long wires. The pMEA is supplied with oxygenated Artificial Cerebrospinal Fluid (ACSF) through bottom perfusion to maintain a controlled environment for the brain tissue during the experiment.

B. Processing Hardware

The Processing hardware uses AMD ZYNQ Z-7030 SoC-FPGA with a carrier card that is connected to a PC using ethernet. Within the Programmable Logic (PL) on the SoC, a SPI interface connects to the Neural Interface modules on the Headstage. Each module has a corresponding Data and Command FIFO that receives the sampled data and sends control commands respectively. The Arm Cortex A-9 core on the Processing System (PS) runs an embedded linux kernel (PetaLinux) that hosts FIFO drivers and paketization logic in C that prepares the data to be sent over UDP packets to the GUI. A FMC connector allows for a parallel path to directly interface the PL to another FPGA or an ASIC to perform pre-silicon and post-silicon tests over a low-latency connection. The PL can also be used for developing closed-loop algorithms in Hardware Description Languages such as Verilog and integrated directly between the Data and Command FIFOs.

C. Graphical User Interface

The GUI offers three functionalities to the system. (1) Displaying recorded data across all channels in real-time, (2)

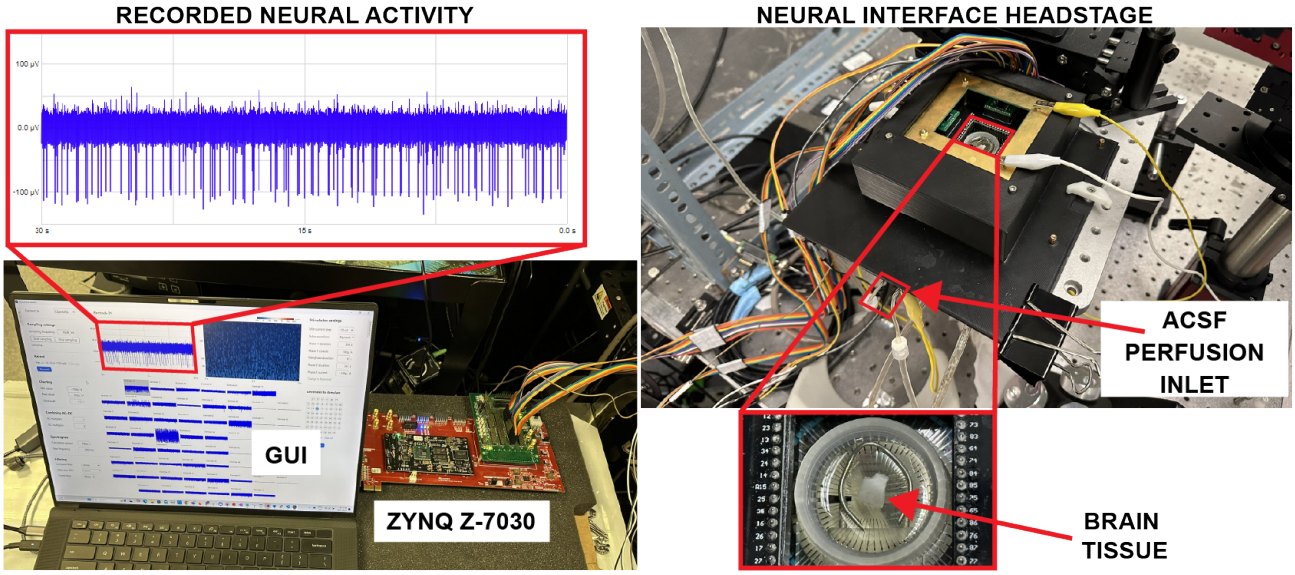

Fig. 3. The experiment setup showing the system with the shielded Neural Interface Headstage, a slice of human brain tissue is placed upon a pMEA, with ACSF provided through bottom perfusion. The setup is placed inside a faraday cage to provide additional shielding with cables connected to the ZYNQ Z-7030 SoC processing hardware. The GUI displays the recorded data showing spiking activity present on one of the channels

Selecting stimulation parameters and custom stimulation protocol modules, and (3) Playback of stored data from previous recordings. ***1. Recording:*** During an experiment, the sampled data is displayed in real-time across all channels. Filters can be applied to it, the time scale and resolution can be adjusted, and a selected channel can be viewed in higher resolution with a spectrogram plot for frequency monitoring. The recorded data is stored in .nwb file format (Neurodata Without Borders [11]), which enables seamless data sharing with collaborators. ***2. Stimulation:*** The user can setup preferred stimulation parameters on the GUI as shown in Fig. 4. In addition to setting the current and duration of each phase, one can select between a single or a series of pulses, the duration between each pulse, and the count of pulse train as desired for an experiment protocol. The stimulation can be applied to any number of channels available by simply selecting the electrode, and triggered by pressing the "Stimulate" button. Using a drop down list, a pre-designed custom stimulation protocol module can be activated that allows additional functionality during experiments. ***3. Playback:*** Post experiment, the user can load a pre-recorded .nwb file and play it on the GUI for quick analysis. The flexibility to add different filters and observe the spectrogram for a channel are available just as they were during real-time recording.

III. Closed-loop Algorithm Development

Our system allows for the development of closed-loop algorithms in several ways. As shown in Fig. 2, We can write software programs in python or C to be run on the PC or on the Arm core of the PS on the ZYNQ Z-7030 chip, or we can convert the algorithms into hardware using HDL like Verilog or VHDL. Each approach has its own advantages. Below section provide more details on each.

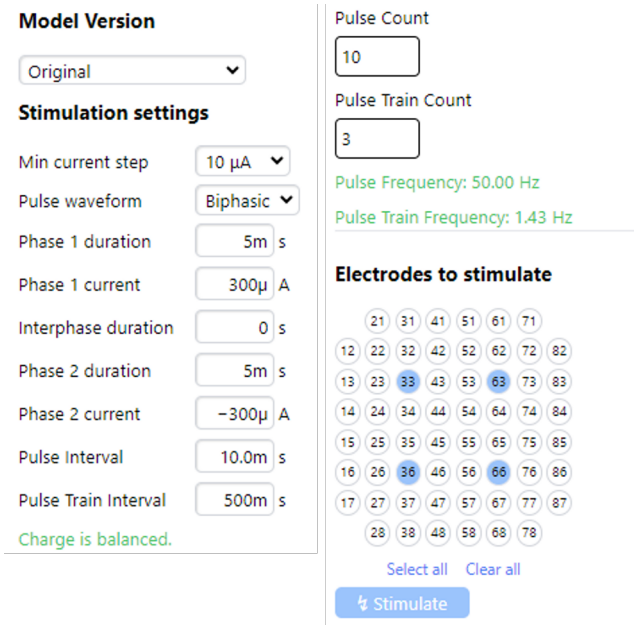

Fig. 4. A snapshot of the Stimulation module showing available settings to setup preferred stimulation parameters

A. Closing the loop in Software

The GUI and software stack was designed to be modular to add additional features as the system evolves. A python backend enables users to integrate custom modules for closed-loop algorithms that can process raw data with <100ms latency. A spike count based algorithm works on selected channels, and triggers stimulation when the firing rate exceeds an upper threshold, or drops below a lower threshold set by the user.

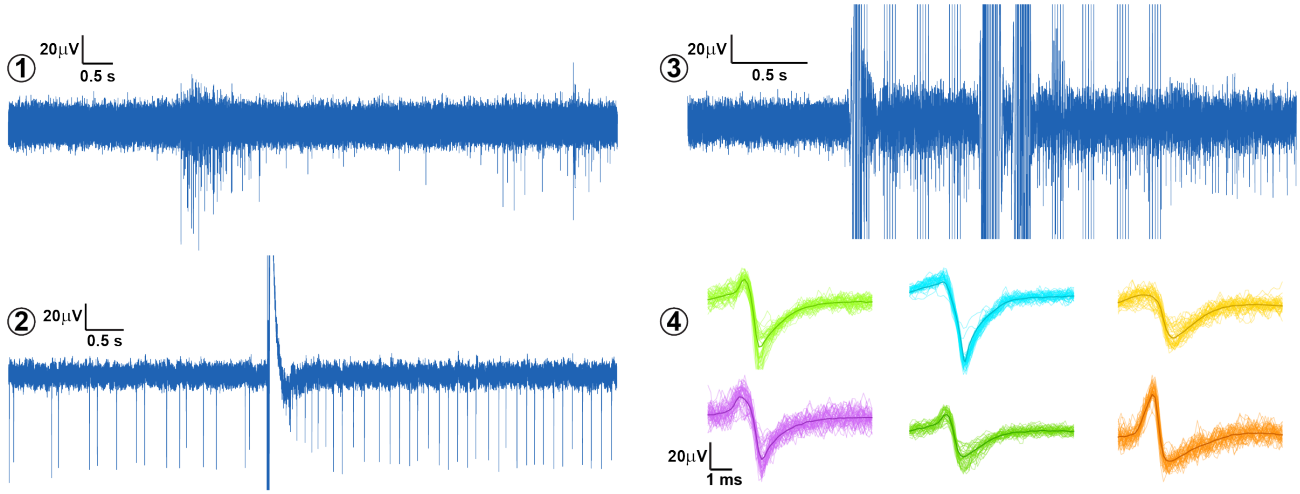

Fig. 5. In-vitro experimental results of recordings conducted from epileptogenic human brain tissue (resected from the temporal lobe) showing spiking activity, and results of neural activity pre- and post- stimulation using different stimulation paradigms. (1) Natural burst of neural activity; (2) Neural activity pre- and post- single pulse coherence stimulation; (3) Neural activity pre- and post- Theta-burst stimulation; (4) Results from spike sorting performed on recorded neural activity.

Spike count post stimulation is monitored to adapt stimulation parameters.

Modules for custom stimulation protocols can be added to the GUI to enable enhanced functionality during experiments. Capabilities to add Theta-burst stimulation [12][13] and Coherence stimulation [14][15] have yielded impressive results, and have shown the usefulness of a platform that can be adapted based on user requirement. Algorithms could also be created in C and run on the Arm Cortex-A9 microprocessor on the ZYNQ Z-7030 SoC. This can improve the latency, while still allowing the flexibility to program in software for rapid prototyping.

B. Closing the loop in Hardware

Using HDL languages such as verilog and VHDL, We can create hardware optimized closed-loop algorithms that interface directly with the Data and Command FIFOs in the PL on the ZYNQ Z-7030, and enable modulation of neural activity with sub-ms latencies. This allows us the flexibility to observe the operation of our algorithm on the GUI and use feedback from neuroscientists to improve its functionality and ensure it does not lead to adverse impacts to the tissue health. This paves the way for translation of the optimized algorithm to an ASIC.

Our system offers the capability to use the FMC connector to interface a fabricated ASIC with a closed-loop neuromodulation algorithm, and perform post-silicon testing and validation before encapsulating the chip for further testing in chronic experiments and eventually in an implantable device.

IV. Results

In-vitro experiments were conducted using our setup shown in Fig. 3 to validate its functionality. Recordings were conducted on epileptogenic brain tissue that was surgically resected from the temporal lobes of human patients a few hours post-surgery. Fig. 5 shows neural activity recorded during different experiments using human brain tissue. Fig. 5 (1) shows naturally occurring burst spiking activity observed while recording baseline data for an experiment. Fig. 5 (2) shows a channel with sparse activity prior to a coherence stimulation with a common parameter across all channels, and the changes observed post stimulation with a marked increase in firing rate. Fig. 5 (3) shows a theta-burst stimulation protocol where the activity prior to stimulation is lower compared to post stimulation, along with observed differences in between pulse trains. Fig. 5 (4) shows results from spike sorting performed on a recorded dataset. Distinct neural spike shapes are observed and showcases the capability of the system to record neural data with a high signal-to-noise ratio (SNR) and low Electromagnetic (EM) noise interference.

V. Conclusion

We present a modular reconfigurable validation platform that can be customized for conducting closed-loop neuromodulation studies for the development of algorithms in software and hardware with translational capabilities towards designing implantable ASICs. Our approach provides us the ability to validate closed-loop algorithms during extensive in-vitro studies using a Microelectrode array. Our solution allows research groups to leverage the expertise available within their groups while allowing a common platform for cross functional collaboration between neuroscientists and ASIC designers. We have presented results from our preliminary studies showcasing the advantages of our system and approach, that takes us closer to accelerating implantable device development as well as exploring new frontiers in neuroscience research.

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References

[1] J. P. Kinney, J. G. Bernstein, A. J. Meyer, J. B. Barber, M. Bolivar, B. Newbold, J. Scholvin, C. Moore-Kochlacs, C. T. Wentz, N. J. Kopell, and E. S. Boyden, "A direct-to-drive neural data acquisition system," *Frontiers in Neural Circuits*, vol. 9, Sep. 2015. DOI: 10.3389/fncir.2015.00046.

[2] R. Wertenbroek, Y. Thoma, F. M. Mor, S. Grassi, M. O. Heuschkel, A. Roux, and L. Stoppini, "SpikeOnChip : A Custom Embedded Platform for Neuronal Activity Recording and Analysis," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 15, no. 4, pp. 743–755, Aug. 2021. DOI: 10.1109/TBCAS.2021.3097833.

[3] J. Park, G. Kim, and S.-D. Jung, "A 128-Channel FPGA-Based Real-Time Spike-Sorting Bidirectional Closed-Loop Neural Interface System," *IEEE Transactions on Neural Systems and Rehabilitation Engineering*, vol. 25, no. 12, pp. 2227–2238, Dec. 2017. DOI: 10.1109/TNSRE.2017.2697415.

[4] G. P. Seu, G. N. Angotzi, F. Boi, L. Raffo, L. Berdondini, and P. Meloni, "Exploiting All Programmable SoCs in Neural Signal Analysis: A Closed-Loop Control for Large-Scale CMOS Multielectrode Arrays," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 12, no. 4, pp. 839–850, Aug. 2018. DOI: 10.1109/TBCAS.2018.2830659.

[5] D. Tsai, D. Sawyer, A. Bradd, R. Yuste, and K. L. Shepard, "A very large-scale microelectrode array for cellular-resolution electrophysiology," *Nature Communications*, vol. 8, no. 1, p. 1802, Nov. 2017. DOI: 10.1038/s41467-017-02009-x.

[6] J. P. Newman, R. Zeller-Townson, M.-F. Fong, S. Arcot Desai, R. E. Gross, and S. M. Potter, "Closed-Loop, Multichannel Experimentation Using the Open-Source NeuroRighter Electrophysiology Platform," *Frontiers in Neural Circuits*, vol. 6, 2013. DOI: 10.3389/fncir.2012.00098.

[7] J. H. Siegle, A. C. López, Y. A. Patel, K. Abramov, S. Ohayon, and J. Voigts, "Open Ephys: An open-source, plugin-based platform for multichannel electrophysiology," *Journal of Neural Engineering*, vol. 14, no. 4, p. 045 003, Aug. 2017. DOI: 10.1088/1741-2552/aa5eea.

[8] J. P. Newman, J. Zhang, A. Cuevas-LÃ³pez, N. J. Miller, T. Honda, M.-S. H. Van Der Goes, A. H. Leighton, F. Carvalho, G. Lopes, A. Lakunina, J. H. Siegle, M. T. Harnett, M. A. Wilson, and J. Voigts, "ONIX: A unified open-source platform for multimodal neural recording and perturbation during naturalistic behavior," *Nature Methods*, vol. 22, no. 1, pp. 187–192, Jan. 2025. DOI: 10.1038/s41592-024-02521-1.

[9] G. O'Leary, A. Gierlach, R. Genov, and T. A. Valiante, "Neural Interface System for Virtual High-Density Microelectrode Array Adaptive Neuromodulation," *2019 IEEE Biomedical Circuits and Systems Conference (BioCAS)*, Nara, Japan: IEEE, Oct. 2019, pp. 1–4. DOI: 10.1109/BIOCAS.2019.8918739.

[10] G. O'Leary, I. Khramtsov, R. Ramesh, A. Perez-Ignacio, P. Shah, H. Moradi Chameh, A. Gierlach, R. Genov, and T. A. Valiante, *OpenMEA: Open-Source Microelectrode Array Platform for Bioelectronic Interfacing*, Nov. 2022. DOI: 10.1101/2022.11.11.516234.

[11] J. L. Teeters, K. Godfrey, R. Young, *et al.*, "Neurodata Without Borders: Creating a Common Data Format for Neurophysiology," *Neuron*, vol. 88, no. 4, pp. 629–634, Nov. 2015. DOI: 10.1016/j.neuron.2015.10.025.

[12] J. Larson and E. Munkácsy, "Theta-burst LTP," *Brain Research*, vol. 1621, pp. 38–50, Sep. 2015. DOI: 10.1016/j.brainres.2014.10.034.

[13] Y. Huang, R. Zelmann, P. Hadar, J. Dezha-Peralta, R. M. Richardson, Z. M. Williams, S. S. Cash, C. J. Keller, and A. C. Paulk, "Theta-burst direct electrical stimulation remodels human brain networks," *Nature Communications*, vol. 15, no. 1, p. 6982, Aug. 2024. DOI: 10.1038/s41467-024-51443-1.

[14] P. Fries, "Rhythms for Cognition: Communication through Coherence," *Neuron*, vol. 88, no. 1, pp. 220–235, Oct. 2015. DOI: 10.1016/j.neuron.2015.09.034.

[15] S. Rich, H. Moradi Chameh, J. Lefebvre, and T. A. Valiante, "Loss of neuronal heterogeneity in epileptogenic human tissue impairs network resilience to sudden changes in synchrony," *Cell Reports*, vol. 39, no. 8, p. 110 863, May 2022. DOI: 10.1016/j.celrep.2022.110863.