32.7 Fascicle-Selective Bidirectional Peripheral Nerve Interface IC with 173dB FOM Noise-Shaping SAR ADCs and 1.38pJ/b Frequency-Multiplying Current-Ripple Radio Transmitter

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The peripheral nervous system (PNS) provides a conduit through which organs can communicate with the central nervous system. PNS neural interfaces have been deployed in open-loop fashion to help restore motor or sensory functions in paralyzed or amputated individuals, and also as implantable closed-loop therapeutic devices for treating chronic medical conditions related to autoimmune or metabolic disorders. Their efficacy and the scope of clinical use, however, are severely curtailed by the invasiveness of the cable, electronics and battery, and the lack of nerve fascicle selectivity and online adaptivity. We present a battery-free wireless PNS interface that features a mm-scale fascicle-selective neural interface IC with extraneural recorders and stimulators, as well as a wearable interrogator with integrated machine learning (ML) to enable adaptive neuromodulation therapy with low invasiveness.

Conventional passive PNS interfaces with tripolar cuff electrode configuration (Fig. 32.7.1, left) suffer from poor fascicle selectivity. Passive high-density flexible nerve cuffs (Fig. 32.7.1, second from the left) improve the selectivity but suffer from EM interference and stimulation crosstalk, and are typically limited to recruiting the superficial nerve fibers. The active probe in [1] (Fig. 32.7.1, second from the right) accesses deeper fascicles by compressing the nerve, so that selective deep-fascicle activation can be achieved by nerve re-shaping. However, deformation is undesirable in vital nerves, such as the vagus nerve, because compression leads to long nerve recovery time and may cause permanent nerve damage when excessive. The presented PNS interface achieves fine deep fascicle selectivity without nerve penetration or compression (Fig. 32.7.1, right). Inspired by a recently discovered method for non-invasive deep brain stimulation [2], it delivers a temporally interfering electric field deep within a nerve without penetrating it by an electrode. This is accomplished by generating two high-frequency stimulation signals at two selected pairs of electrodes in the high-density cuff electrode array with a small frequency difference of Δf, with Δf arising as the frequency of the resulting interference envelope. Since nerves are responsive in a low-frequency band where Δf resides, one can activate the desired deep fascicles without affecting most other fascicles in the nerve. In the presented configuration, the miniaturized PNS interface IC is attached to the rigid base of a high-density flexible cuff electrode array to minimize EM interference.

Figure 32.7.2 (left) illustrates the block diagram of the presented IC that includes: (1) an array of 64 neural analog-to-digital converters (ADCs) and electrical stimulators, for high-density neural activity monitoring and for temporally-interfering focal stimulation, respectively; (2) a wireless data transmitter (TX) and a clock generator, for uploading recorded data and for generating clock signals on-chip, respectively; (3) a wireless power management unit (PMU) and data receiver (RX), receiving ultrasound power and commands, respectively; and (4) a RISC-V processor for on-chip data handling and processing. Figure 32.7.2 (right) shows the interrogator comprised of: (1) a decimation filter followed by a channel scanner for neural data pre-processing; (2) a convolutional neural network (CNN) for real-time neural pathway classification; and (3) a finite-state-machine (FSM) that controls the ultrasound power/data transmitter for closed-loop operation.

As illustrated in Fig. 32.7.3 (left, top), neural amplifiers conventionally use either the bipolar or the more popular unipolar configuration, which typically suffer from large number of electrodes or from imbalanced input impedance significantly degrading the CMRR, respectively. To maintain the minimum number of electrodes and a moderate PNS-suitable CMRR, we introduce a pseudo-differential configuration with matched input impedance by using an additional preamplifier for the reference input. Each preamplifier is a switched-capacitor correlated-double-sampling amplifier (CDSA) that reduces low-frequency noise and offset as shown in Fig. 32.7.3 (left, bottom). A source-follower buffers the CDSA's input and sets the low-pass frequency corner. An inverter self-biased near the cut-off region replaces a conventional OTA to reduce static power consumption. A 1st-order noise-shaping (NS) SAR ADC with an inverter-based integrator samples the pre-amplified neural signal and reference differentially to enable common-mode rejection, as depicted in Fig. 32.7.3 (left, middle). During phase P1, the CDSAs amplify the potential difference between the neural signal and the reference, which is then buffered on the ADC's sampling capacitors; during phase P2, the CDSAs sample the dynamic offset and the low-frequency noise, while the ADC converts the sampled signal through P1 to a digital code using asynchronous SAR logic. Dynamic element matching (DEM) is employed to reduce the impact of the mismatch in the capacitor bank. The front-end achieves an input-referred noise of $2.2\mu V_{rms}$ over 2.5kHz with NEFs of 2.55 and 3.93, without and with the ADC power included, respectively. The ADC achieves an ENOB of 14b and a Schreier FOM of 173dB.

Figure 32.7.4 (left) introduces the frequency-multiplying current-ripple data TX. It employs a ring-oscillator (RO) as its core frequency generator for OOK modulation that is attained via a power-modulator in the power amplifier bias path. To reduce the power, we exploit the nature of the power-supply current in an inverter chain. The sequential switching of each inverter stage gives rise to a train of equally spaced current spikes. When combined to fit into one time period of the ring oscillator, these current spikes result in a high-frequency switching harmonic of an integer value equal to the number of stages, N. In other words, the RO supply current I_A spikes at a frequency f_A which is N times higher than the RO oscillation frequency, yielding the corresponding power savings. The RO oscillation center frequency is calibrated and controlled by a programmable on-chip LDO. The data TX consumes only 27.63μW when transmitting at 20Mb/s, demonstrating 1.38pJ/b energy efficiency.

The IC is compatible with ultrasonic energy harvesters, with energy supplied wirelessly through the skin. An ultrasound power receiver was connected to the power and data receiving circuits as shown in Fig. 32.7.4 (right). In the power path, a full-wave bulk-biased passive rectifier is followed by an LDO bank. A data receiver recovers ASK modulated data. The power-shaping circuits (rectifier and LDO combined) operate with 70% power conversion efficiency for the nominal load of 480μW.

The IC has been validated in vivo in a sciatic nerve recording from an anesthetized rat. A flexible 8×8-contact polyimide microelectrode array was implanted over the sciatic nerve and connected to the IC. Figure 32.7.5 (top, right) shows how the IC tolerates an electrical stimulation artifact when recording EMG at one of the microelectrodes. Figure 32.7.5 (left) depicts recordings by the IC of compound action potentials naturally evoked by three rat paw actions: dorsiflexion, plantarflexion and heel prick, which engage distinct neural pathways. These recordings are transmitted from the IC to the in-the-loop neural pathway classifier realized in the wearable digital interrogator. As depicted in Fig. 32.7.5 (bottom, right), first, the channel scanner sequences the 8×8 digital neural data both longitudinally and transversely to emphasize spatial and temporal features, respectively. Next, the two resulting feature maps are fed into the CNN that is trained to classify the three sensory stimuli. As shown, the classifier exhibits a good accuracy of 86.7% from a 3-fold dataset from one animal, when realized on a low-power 500μW FPGA. This implementation reduces the number of the CNN model parameters by a factor of 420× compared to [3] while F1-score drops by only 0.029.

We have also experimentally demonstrated PNS fascicle selectivity in neural stimulation by the temporal interference method, both in vitro and in vivo, building on the previous demonstration in the rodent brain [4]. Figure 32.7.6 (top) features the in vitro validation with a cuff in a saline bath, with Δf=10Hz. The 10Hz interference voltage envelope deeper in the cuff is larger than on the surface confirming that deeper fascicles can be selectively targeted. Figure 32.7.6 (bottom) depicts a demonstration of temporal interference in vivo, where four different movements of a rat's hindlimb were elicited by applying stimulation at distinct electrode contact pairs, with the activity threshold of 2V.

The chip micrograph, die-on-board packaging example and a comparison table are depicted in Fig. 32.7.7. A broad range of applications of this work is envisioned, holding promise for the ultimate use in adaptive therapies for neuromodulation in vital nerves such as the vagus nerve, for treating intractable autoimmune and inflammatory diseases.

References:

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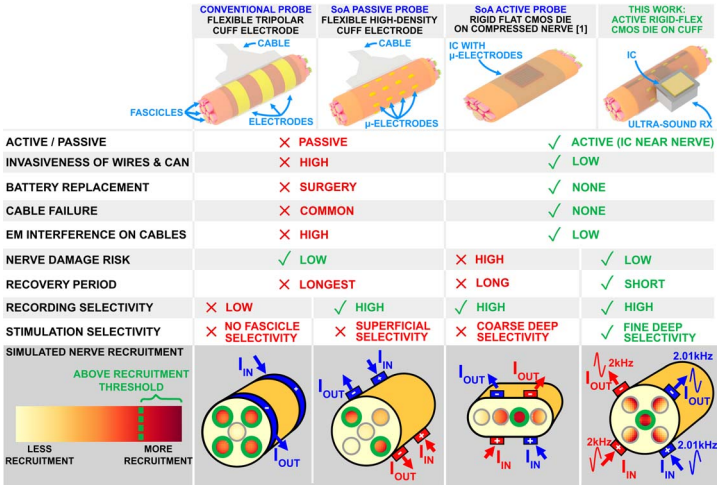


Figure 32.7.1: Comparative analysis of peripheral nerve electrical interfaces.

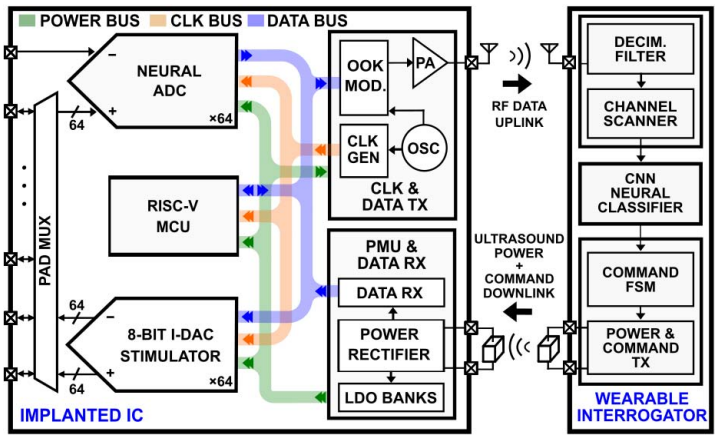


Figure 32.7.2: Block diagram of peripheral nerve interface IC and external interrogator.

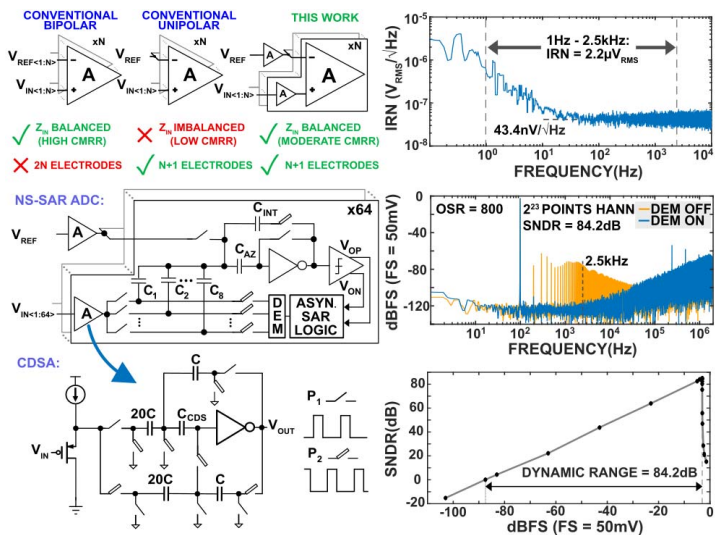


Figure 32.7.3: Neural ADC front-end and its experimentally measured results.

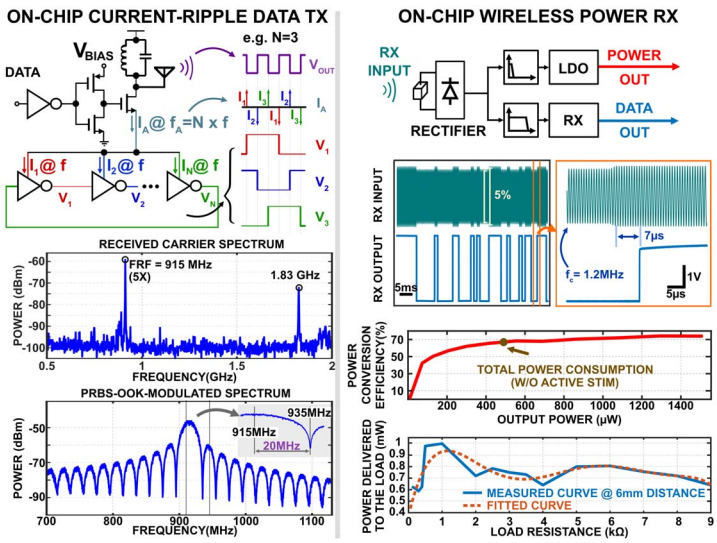


Figure 32.7.4: Frequency-upconverting data transmitter, wireless data/power receiver and their experimentally measured results.

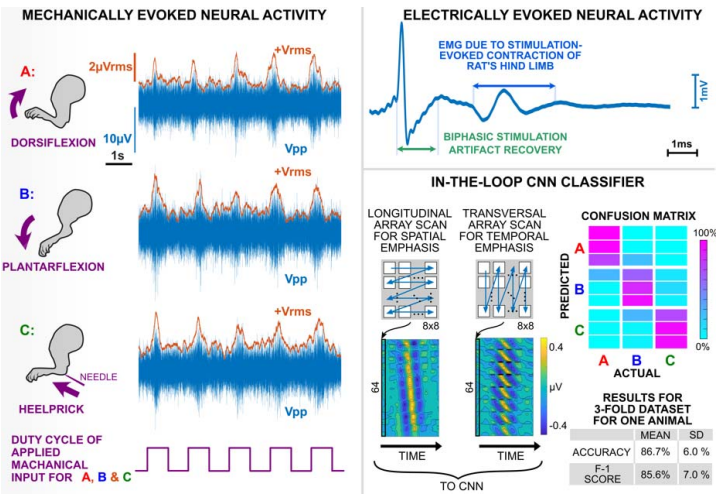


Figure 32.7.5: Experimentally measured evoked rodent sciatic nerve activity and its classification by in-the-loop CNN inference engine.

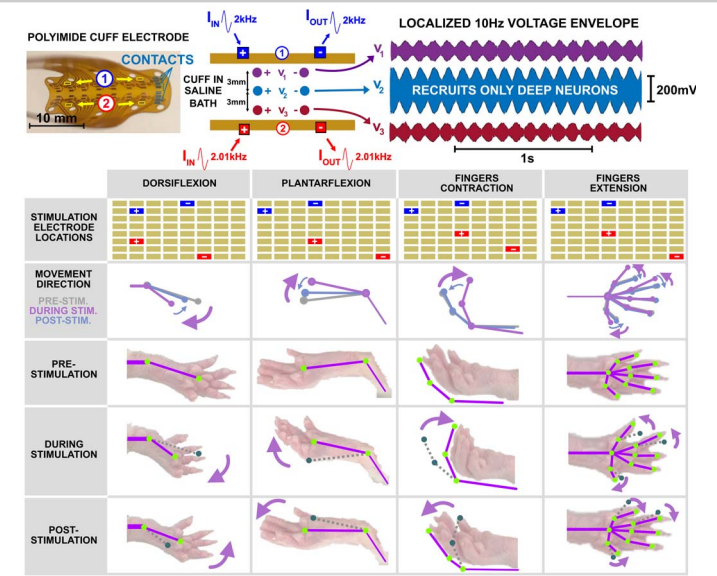
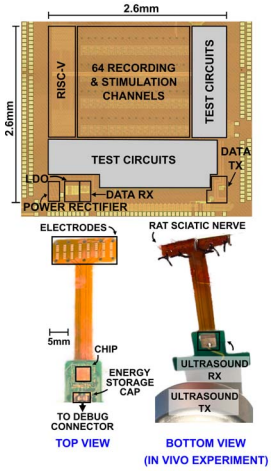


Figure 32.7.6: Experimental in vitro (top) and rodent in vivo (bottom) validation of fascicle-selective stimulation.



	THIS WORK	ISSCC 21 [1]	TCAS-I 21 [5]	JSSC 19 [6]	JSSC 17 [7]
SYSTEM					
WIRELESS POWER	YES	YES	NO	YES	NO
TECHNOLOGY (nm)	65	130	180	180	40
SUPPLY VOLT. (V)	0.4-2.5	0.5-1.6	1.8	1.2/1.8	1.2
TOTAL POWER (µW)	480	810	418.14*	2300	17
AREA (mm^2)	5.00	7.02	1.65	7.82	-
NO. REC/STIM CH.	64 / 64	64 / 1	1 / N/A	10 / N/A	1 / N/A
AFE					
AREA/Ch (mm^2)	0.02	0.01	1.65	-	0.014
POWER/Ch (µW)	5.2	0.14	418.14*	37.6	17
IRN (μV_{rms})	2.2	24.7	-	1.9	2.26*
BW (kHz)	2.5	10	1	5.5	5
NEF (W/O ADC)	2.55	N/A	N/A	4	N/A
NEF (WITH ADC)	3.93	4.7	11.2	N/A	4.71*
INPUT IMPED. (GΩ)	>1	0.1	-	-	0.07
CMRR (dB)	69	-	140	-	-
DYN. RANGE (mV_{pp})	50	25	60	-	8
SNDR (dB)	84.2	49.92*	-	48.76*	61.85
FOM_W (fJ/Conv.Step)[3]	71.5	27	3309*	-	1680
FOM_S (dB)[2]	173.4	165.1	159.7*	-	146.5
TX					
POWER (µW)	27.63^	330*^	N/A	N/A	N/A
DATA RATE (Mbps)	20	-	N/A	3	N/A
ENERGY EFF. (pJ/bit)	1.38	-	N/A	-	N/A
STIM					
RANGE (µA)	8 - 2000	5-200	N/A	N/A	N/A
COMPLIANCE V. (V)	3.3V	1.8V	N/A	N/A	N/A

*: ESTIMATED N/A: NOT APPLICABLE -: NOT AVAILABLE [1]: ADC ONLY
^: AT MAX DATA RATE FOM_W:(fJ/ConvStep) = POWER / (2^{ENOB} X 2BW)
FOM_S:(dB) = SNDR +10log(BW/POWER)

Figure 32.7.7: Die micrograph, die-on-board packaging example and comparison table.

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