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Advanced Noise-Shaping SAR ADCs Utilizing Single-Capacitor Arbitrary-Resolution DACs for Miniaturized Neural Interfaces

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***Abstract*—This paper presents the development and validation of a high-performance Noise-Shaping (NS) Successive-Approximation-Register (SAR) Analog-to-Digital Converter (ADC) specifically tailored for low-power, high-density Implantable Neural Interfaces (INIs). The proposed design introduces a novel approach to the Digital-to-Analog Converter (DAC) formation within the NS-SAR ADC, utilizing a single capacitor to achieve arbitrarily-high resolution. It minimizes distortion due to mismatches of conventionally used capacitor banks and reduces the NS-SAR ADC area, enabling higher resolution without a proportional increase in area. Furthermore, our design addresses the challenges of kickback noise and lossy integration, improving overall performance and signal integrity during the conversion process. Simulation and experimental results substantiate the performance of the proposed noise-shaping SAR ADC. The ADC demonstrated a high peak signal-to-noise-and-distortion ratio (SNDR) of 89 dB. Moreover, it proved its robustness across different frequencies and capacitor mismatches, maintaining an SNDR of 70dB even with a 10% mismatch of the capacitors.**

***Index Terms*—Implantable Neural Interfaces, Noise-Shaping, Analog-to-Digital Converter, Digital-to-Analog Converter**

I. Introduction

Implantable Neural Interfaces (INIs) are transformative technologies with significant potential for advancing the treatment of neurological disorders [1]–[3], restoring impaired functions [4]–[6], and facilitating direct communication between the human brain and external devices.

The performance of INIs hinges significantly on a spectrum of specialized components, a crucial one being the ADC. Most traditional ADCs [7], despite their utility, are plagued by substantial issues. For example, Successive-Approximation-Register (SAR) ADCs [8], characterized by their Nyquist sampling, offer faster conversion rates but struggle to achieve high resolution. On the other hand, oversampling ADCs, such as $\Delta\Sigma$ ADCs, can attain respectable resolution at the cost of reduced speed [5], [6], [9]–[12]. To address these challenges, the Noise-Shaping (NS) SAR ADC has been developed [4], [13]. This novel approach blends the strengths of both SAR ADC and $\Delta\Sigma$ ADC, effectively mitigating the problems of excessive power consumption and quantization noise. Consequently, the NS-SAR ADC is emerging as a highly suitable option for use in implantable neural interfaces.

Figure 1(a) presents a generic NS-SAR ADC circuit diagram, with the SAR ADC components accentuated in yellow. The SAR ADC operates by assessing the difference between

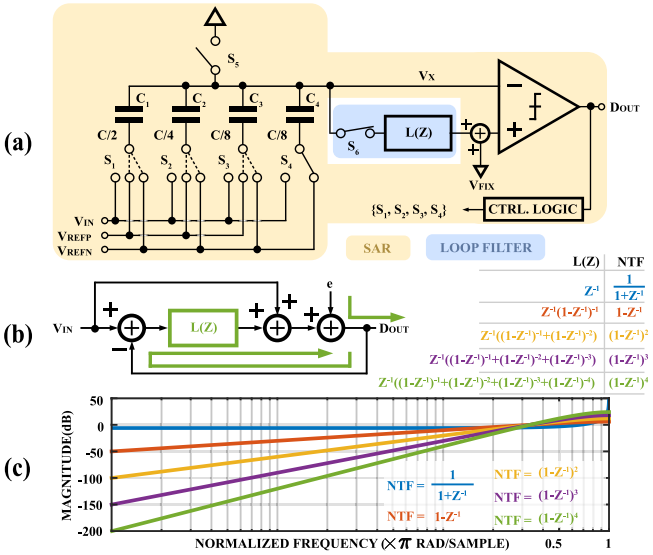

Fig. 1. A generic noise-shaping SAR ADC illustration. (a) Simplified circuit diagram of a noise-shaping SAR ADC. (b) Block diagram of the noise shaping SAR ADC in z-domain. (c) Quantization noise transfer function plots for different ADC orders.

the input and the reference signals generated by a DAC, contrasting this difference against a static reference signal. A binary search algorithm is integrated into this process, facilitating rapid conversion by identifying the smallest difference between the input and the reference signals. However, the confined resolution of the reference signal, as produced by a DAC, incurs quantization errors. These errors manifest as white noise, permeating the full bandwidth of the ADC. The loop filter, $L(Z)$, highlighted in blue in Fig. 1(a), serves as a cornerstone of the NS-SAR ADC. Upon each SAR ADC conversion, this filter collects and manipulates the quantization errors, which are then added to the subsequent SAR ADC conversion. This treated residual voltage acts in a manner comparable to an offset voltage. As presented in the z-domain signal flow diagram in Fig. 1(b), the quantization noise undergoes processing by a high-pass filter formed by loop filter and negative feedback path highlighted in green, thereby purging the system of low-frequency quantization errors. This leads to a superior signal-to-quantization-noise-and-distortion ratio (SNDR), most notably when the signal

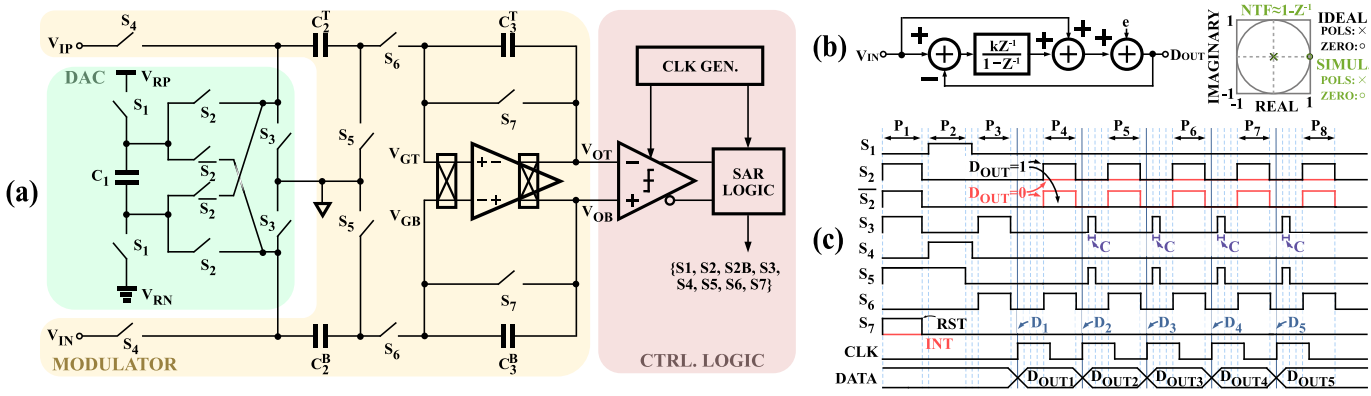

Fig. 2. The presented noise-shaping SAR ADC illustration. (a) Circuit diagram of the presented noise-shaping SAR ADC. (b) Block diagram of the noise shaping SAR ADC in z-domain. (c) Timing diagram of the clocks and SAR logic.

bandwidth is significantly lower than the NS-SAR ADC's sampling frequency. Figure 1(b)&(c) illustrate the transfer function of the high-pass filter, revealing that diverse $L(Z)$ configurations yield different high-pass filter orders, thereby repressing low-frequency quantization noise. Nevertheless, the SNDR of standard NS-SAR ADCs is constricted by distortion due to capacitor bank mismatches. Expansion of the capacitor bank's area could attenuate the mismatch effects, but concurrently, it will inflate the ADC's area, thus reducing the recording channel density per given area. Techniques like dynamic element matching or off-chip calibration can also curtail mismatch effects, but they require additional circuitry or extensive testing. Additional issues, such as kickback noise and charge loss prompted by parasitics at the comparator's input, can further degrade the ADC's SNDR.

To effectively address these issues, we propose a NS-SAR ADC that employs a single capacitor to construct an arbitrarily high-resolution DAC for input voltage referencing. The proposed design overcomes the limitations discussed above, offering a robust, energy-efficient, and compact solution that is more suitable for INIs.

II. Proposed NS-SAR ADC Design

This section presents the architecture of the proposed noise-shaping SAR ADC, a design that presents marked improvements over conventional NS-SAR ADCs. The proposed design emphasizes significant advancements in noise reduction, space efficiency, and cost-effectiveness, making it a noteworthy contender in the realm of high-performance ADC, particularly suitable for INIs, as supported by the following points.

1) Capacitor Mismatch and Area Efficiency: The simplified schematic of the proposed NS-SAR ADC, shown in Fig. 2(a), uses a single capacitor to construct an arbitrary-resolution DAC, highlighted in green. This streamlined configuration mitigates distortion from capacitor bank mismatches while achieving arbitrarily high resolution via charge sharing with feedback capacitors on the integrators' feedback path. Moreover, the compact single capacitor-based DAC optimizes the NS-SAR ADC's area use, fostering a higher resolution without the requisite increase in area.

2) Control of Kickback Noise and Lossy Integration: Noise-shaping ADCs typically grapple with the twin challenges of kickback noise and lossy integration, which mostly arise from the parasitic capacitors located at the comparators' input. Our proposed design astutely counteracts these problems by integrating a specially designed modulator, as highlighted in yellow in Fig. 2(a). This modulator's role is to integrate the residue voltage. The modulator concurrently drives the comparator, as highlighted in pink in Fig. 2(a). Here, the majority of kickback noise from the comparator is redirected to the OTA rather than the integrating capacitors, thereby significantly maintaining accurate charge on these capacitors, (C_3^{T} and C_3^{B}). This configuration also minimizes the charge loss at the comparator's input by enabling the OTA to charge the parasitic capacitance V_{OT} and V_{OB} nodes rather than allowing these parasitic capacitors to draw charge from the integrating capacitors. These combined efforts result in amplified signal integrity and enhanced overall performance throughout the ADC conversion process.

3) Noise Transfer Function (NTF): The z-domain signal block diagram of our proposed ADC is showcased in Fig. 2(b, left), illustrating a first-order cascade-integrator-feed-forward NS-SAR ADC. It is worth noting that the ideal NTF zero is conveniently positioned on the unity circle (z = 1), allowing for impeccable in-band noise suppression. In the proposed design, the location of the nonideal zero is primarily influenced by the finite dc gain of the Operational Transconductance Amplifier (OTA), resulting in a slight inward shift of the zero. Importantly, this shift has minimal impact on the overall transfer function, enabling the realization of a sharp NTF. Despite the nonideal characteristics introduced by the OTA, the resulting ADC design maintains its noise suppression capabilities and preserves the accuracy of the acquired signals.

4) Noise Reduction: The proposed design integrates a chopper that effectively suppresses the flicker noise generated by the OTA, significantly reducing the ADC's overall noise floor and delivering a remarkably clear and accurate output signal.

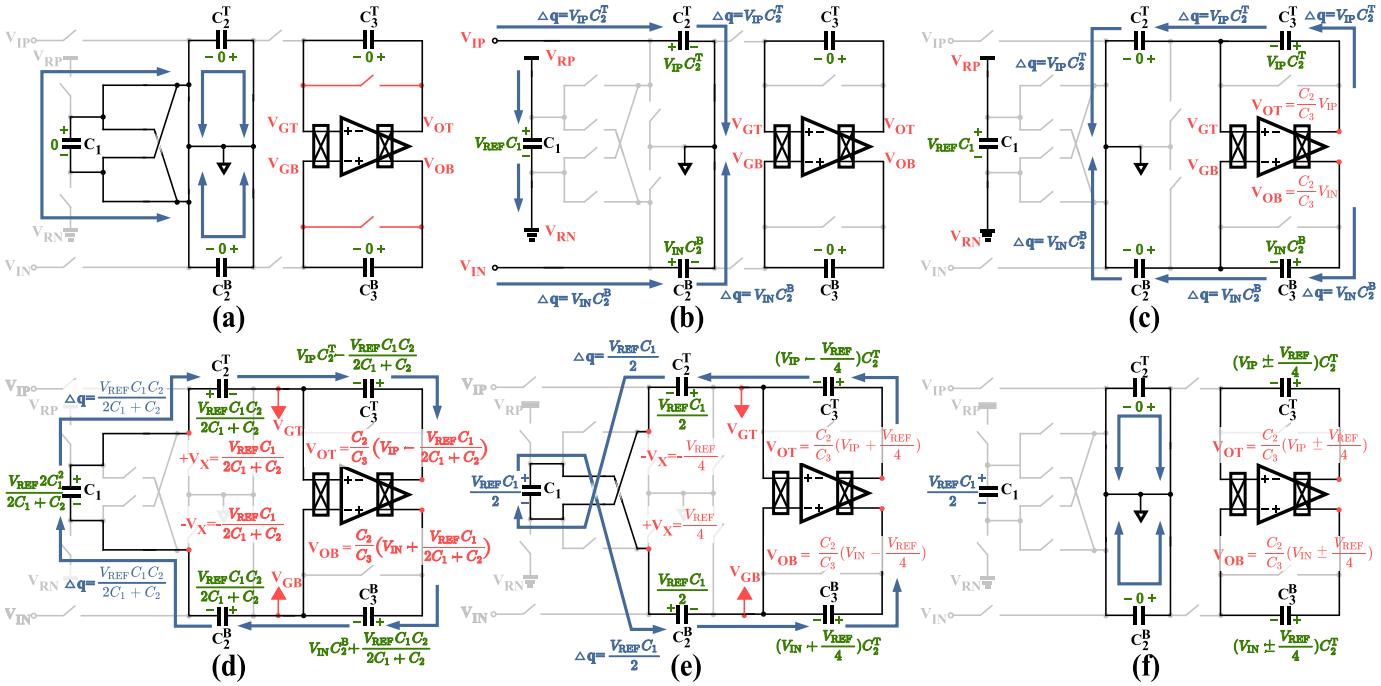

Fig. 3. Key operation phases of the presented noise-shaping SAR ADC: (a) reset, (b) sampling, (c) integration, (d) charge redistribution for MSB ='1', (e) charge redistribution for MSB ='0', and (f) charge dumping.

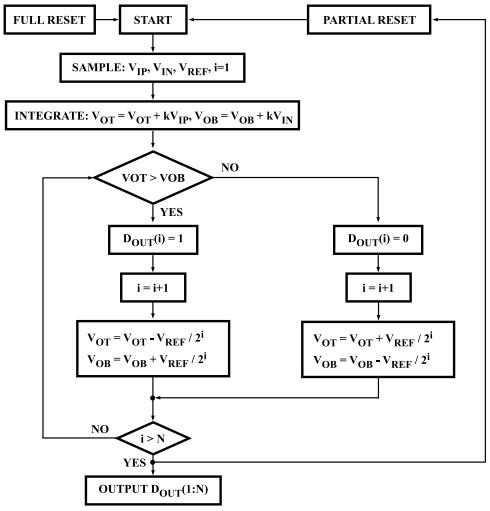

Fig. 4. Flow chart illustrating the sequence of operations in the presented noise-shaping SAR ADC, including sampling, integration, charge redistribution, and reset phases.

5) Clock and SAR Logic: The energy-efficient SAR logic and clock generation, depicted in Figure 2(c), provide the clock signal for the proposed NS-SAR ADC for rapid conversions. Section III offers a detailed analysis of the proposed NS-SAR ADC.

III. Operational Phases of the Proposed NS-SAR ADC

Figure 3 depicts the proposed NS-SAR ADC's operation, outlining the various phases: reset, sampling, integration, charge redistribution, and charge dumping. Each phase's migrated charge, residual charge on each capacitor, and node voltage values are highlighted in blue, green, and red, respectively.

The reset phase, represented in Fig. 3(a), aligns with the P_1 period in Fig. 2(c). During this phase, capacitors C_1, C_2^{T}, and C_2^{B} discharge. If the circuit powers up initially or stays idle for a prolonged duration, capacitors C_3^{T} and C_3^{B} self-discharge to their virtual ground nodes, V_{GT} and V_{GB}, to eliminate any uncertain charges. Conversely, during typical operation, switch S_7 remains open, thus preserving the charges on C_3^{T} and C_3^{B}.

Fig. 3(b) and (c) demonstrate the sampling and integration phases, respectively. During the sampling phase (P_2 in Fig. 2(c)), the input voltages, V_{IP} and V_{IN}, are sampled on the left plates of C_2^{T} and C_2^{B}, respectively, while concurrently C_1 samples the reference voltage, $V_{\mathrm{REF}} = V_{\mathrm{RP}} - V_{\mathrm{RN}}$. Following this, the integration phase transpires (P_3 in Fig. 2(c)). Here, capacitors C_2^{T} and C_2^{B} discharge their left plates to ground, causing the right plates of C_3^{T} and C_3^{B} to extract a same amount of charges from the OTA. As a result, the OTA's output voltages, V_{OT} and V_{OB}, align proportionally to the input voltages.

Upon the integration phase's completion, the comparator activates to decide the MSB, checking if V_{OT} surpasses V_{OB}. If MSB =1, the circuit configures as displayed in Fig. 3(d), representing the charge redistribution phase (P_4 in Fig. 2(c)). Here, the previously stored charge on C_1 redistributes among C_1, C_2^{T}, and C_2^{B}, causing V_{OT} to subtract a portion of V_{REF}, and V_{OB} to add the same portion of V_{REF}. If $C_1 = C_2^{\mathrm{T}}/2$, then $V_X = V_{\mathrm{REF}}/4$, the charge transferred to C_2^{T}'s left plate equals

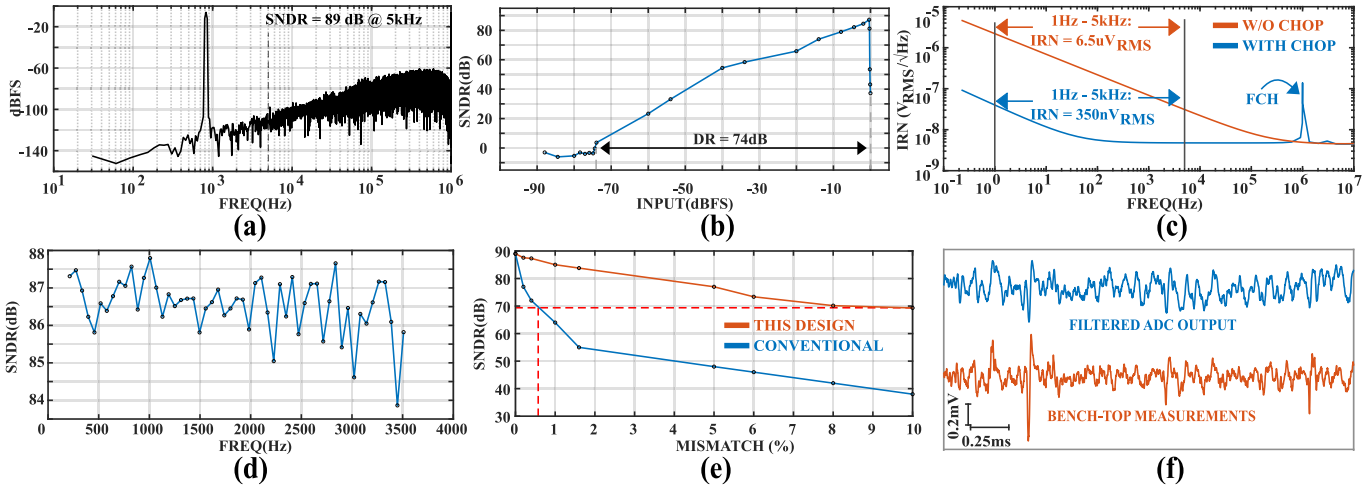

Fig. 5. Simulation and experimental measurement results: (a) Simulated signal-to-noise-and-distortion ratio (SNDR), (b) Simulated SNDR vs. the input amplitude. (c) Simulated input-referred-noise (IRN) with and without chopping. (d) Simulated SNDR vs. input frequency. (e) Simulated SNDR vs mismatch. (f) Experimentally measured LFP vs a bench-top instrument reference.

$V_{\mathrm{REF}}C_2^{\mathrm{T}}/4$, leading to an equivalent charge leaving from C_3^{T}'s right plate and causing a $V_{\mathrm{REF}}/4$ shift in the OTA's output voltage. Fig. 3(e) can be analyzed similarly, representing the charge redistribution phase when the MSB is '0'. After either Fig. 3(d) or (e), the comparator is engaged again to determine the second bit. Before commencing the subsequent charge redistribution phase, the charge dumping phase shown in Fig. 3(f) is performed to eliminate charges on C_2^{T} and C_2^{B}.

In summary, the operations of the proposed NS-SAR ADC are encapsulated in the flow diagram in Fig. 4. A full reset is initiated to clear all charges on each capacitor. Subsequently, the circuit begins its operation by first sampling the input and reference voltages, then integrating the input voltage into the integrator with a gain defined by the ratio of C_2^{T} to C_3^{T}, while setting i to 1. The comparator then ascertains the MSB value, and the digital output $D_{\mathrm{OUT}}(i)$ is stored in the register. The output voltage of the integrator is updated through charge redistribution. If the desired resolution during the SAR conversion, N, is achieved, the output data $D_{\mathrm{OUT}}(1:N)$ is produced and the quantization error is integrated into the next cycle. A partial reset is then performed before repeating the process from the beginning.

IV. Simulation and Experimental Results

Figure 5 shows simulation and experimental measurement results that comprehensively evaluate our system's performance, covering critical aspects such as SNDR, input-referred noise, frequency response, mismatch, and real-world validation. The depth and breadth of these results affirm the reliability and robustness of the presented ADC.

Figure 5(a) displays a Fast Fourier Transform (FFT) plot with 2^{16} points, employing a Hanning window for the ADC output with a -6dBFS sinusoidal input. This graph demonstrates that at the critical frequency of 5kHz, within which the majority of neural signal residues reside, our ADC achieves a peak SNDR of 89dB. Fig. 5(b) presents SNDR of the proposed NS-SAR ADC against the input amplitude, illustrating the ADC's dynamic range of 74dB. This range highlights the ADC's proficiency in accurately processing a wide spectrum of neural signals. In Fig. 5(c), a comparison of the ADC's input-referred noise with and without chopping is exhibited. Evidently, the utilization of chopping drastically diminishes the ADC's input-referred noise from $6.5\mu V_{\mathrm{RMS}}$ to a mere $300nV_{\mathrm{RMS}}$. Fig. 5(d) displays the ADC's SNDR against the input frequency, thus underlining the ADC's consistency across various bandwidths of neural signals. Further evidence of the ADC's robustness is demonstrated in Fig. 5(e), which showcases the SNDR against the ADC's capacitor mismatch. Notably, the ADC sustains an SNDR of 70dB, even with a 10% mismatch. This superior performance significantly overshadows that of a conventional NS-SAR ADC, which require less than 1% mismatch for the same SNDR performance. Lastly, Fig. 5(f) provides in vivo experimental results, affirming that the proposed NS-SAR ADC's performance aligns with benchtop measurements.

Collectively, these results validate the resilience, noise tolerance, and overall performance of the proposed design, thereby underscoring its potential for high-performance analog-to-digital conversion in the realm of INIs.

V. Conclusion

This paper presents a novel NS-SAR ADC design with improved noise reduction, area utilization, and cost-effectiveness. It effectively addresses common challenges in conventional NS-SAR ADCs, such as capacitor mismatch, kickback noise, and lossy integration. By strategically positioning a DC zero and incorporating a chopper, the design achieves optimal low-frequency performance and suppresses flicker noise. Its compact and efficient nature makes it suitable for high-performance ADC applications, particularly in the context of INIs.

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